PATENT APPLICATION

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of

YAMASAKI, KOZO, et al.

Docket No: Q57368

Appln. No.: 09/471,332

Group Art Unit: 2827

Confirmation No.: 7276

Examiner: Norris, Jeremy C.

Filed: December 23, 1999

For: MULTILAYER-WIRING SUBSTRATE AND METHOD FOR FABRICATING SAME

AMENDMENT UNDER 37 C.F.R. § 1.111

Commissioner for Patents
Washington, D.C. 20231

Sir:

Responsive t the outstanding Office Action of July 3, 2002, three times extended from October 3, 2002 to January 3, 2003, by the filing of an appropriate petition and payment for extension of time submitted herewith, please amend the above-identified application as follows:

IN THE CLAIMS:

Please cancel claims 13-17 without prejudice or disclaimer.

The claims are amended as follows:

1. (Twice amended) A multilayer-wiring substrate comprising:

a first wiring conductor with a recessed surface formed by etching a surface of the first wiring conductor,

a first insulating layer formed on a surface of the first wiring conductor except over the recessed surface so that a first via-hole penetrates through the first insulating layer to the recessed surface; and

a second insulating layer formed on the other surface of the first wiring conductor, wherein a depth of the recessed surface is 5-30% of the thickness of the wiring conductor, and said conductor comprises copper.

5. (Twice amended) A multilayer-wiring substrate comprising:

a first wiring conductor having top and bottom surfaces; a first insulating layer formed on the top surface of the first wiring conductor; a first via-hole penetrating through the first insulating layer; and a first columnar via-conductor formed in the via-hole,

wherein the first wiring conductor has a first recessed surface formed at the top surface of the first wiring conductor so that a bottom end of the first columnar via-conductor contacts the first recessed surface of the first wiring conductor, a depth of the recessed surface is 5-30 % of the thickness of the wiring conductor, and said conductor comprises copper.

Please add new claims 18-21 as follows:

18. (New) A method for fabricating a multilayer-wiring substrate having a via-conductor in a via-hole, said multilayer-wiring substrate comprising:

a wiring conductor with a recessed surface formed by etching a surface of the wiring conductor,

a first insulating layer formed on a surface of the wiring conductor except over the recessed surface so that a via-hole penetrates through the insulating layer to the recessed surface;

a via-conductor plated on an inner peripheral wall of the via-hole and extendingly plated on the recessed surface of the wiring conductor that forms a bottom of the via-hole; and

a second insulating layer formed on the other surface of the wiring conductor, wherein a depth of the recessed surface is 5-30% of the thickness of the wiring conductor, and said conductor comprises copper,

said method comprising:

forming an insulating layer on a wiring conductor comprising copper;

forming a via-hole in the insulating layer by removing the insulating layer to an extent that the insulating layer in the via-hole becomes fragmented and adheres to the wiring-conductor located at the bottom of the via-hole;

then etching the wiring conductor located at the bottom of the via-hole so that the fragments are removed and a recessed surface is formed in an amount of 5-30% of the thickness of the wiring conductor;

then forming a via-conductor in the via-hole by plating a metal on an inner peripheral wall of the via-hole and extendingly plating the metal on the recessed surface of the wiring conductor; and

forming a second insulating layer on the other surface of the wiring conductor.

19. (New) A method for fabricating a multilayer-wiring substrate having a via-conductor in a via-hole as clamed in claim 18, further comprising:

etching an inner peripheral wall of the via-hole that penetrates the insulating layer before etching the wiring conductor located at the bottom of the via-hole.

20. (New) A method for fabricating a multilayer-wiring substrate, said multilayer-wiring substrate comprising:

a wiring conductor having top and bottom surfaces;

an insulating layer formed on the top surface of the wiring conductor;

a via-hole penetrating through the insulating layer; and

a columnar via-conductor formed in the via-hole,

wherein the wiring conductor has a recessed surface formed at the top surface of the wiring conductor so that a bottom end of the first columnar via-conductor contacts the recessed surface of the wiring conductor, a depth of the recessed surface is 5-30% of the thickness of the wiring conductor, and said conductor comprises copper,

said method comprising the steps of:

forming a photosensitive resin layer on a wiring conductor comprising copper;

exposing the photosensitive resin layer and then developing to form a via-hole therein;

chemically etching resin at a surface of the photosensitive resin layer and resin at an inner wall of the via-hole;

chemically etching a surface of the wiring conductor exposed at a bottom of the via-hole so as to form a recessed surface in an amount of 5-30% of the thickness of the wiring conductor; and

forming a via-conductor in the via-hole by plating a metal on an inner peripheral wall of the via-hole and extendingly plating the metal on the recessed surface of the wiring conductor.

21. (New) A method for fabricating a multilayer-wiring substrate as claimed in claim 20, wherein said developing comprises holding the multilayer-wiring substrate substantially

horizontally and turning the substrate upside down during the development so that a via-hole axis is formed perpendicular to the recessed surface of the wiring conductor.

REMARKS

In response to the rejection under 35 U.S.C. § 112, second paragraph, claims 1 and 5 have been amended in accordance with the Examiner's suggestion to replace "the recess" with "the recessed surface". Withdrawal of the rejection is respectfully requested.

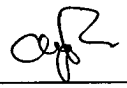
Applicants note that the elected claims are otherwise allowable over the prior art of record. Non-elected claims 13-17 have been canceled. Applicants present herein new claims 18-21 in which the method steps have been modified to conform with the allowable product claims. Claim 18 corresponds to original claim 13, whereas claim 20 corresponds to original claim 15. New claims 18-21 include all of the limitations of the allowable product claims. Applicants respectfully request the Examiner to enter method claims 18-21 under the rejoinder provisions of MPEP §821.04. New method claims 18-21 which include all of the limitations of the allowable product claims should also be allowable over the prior art of record.

Allowance of claims 1-10 and 18-21 is earnestly solicited.

In the event that the Examiner believes that it may be helpful to advance the prosecution of this application, the Examiner is invited to contact the undersigned at the local Washington, D.C. telephone number indicated below.

The USPTO is directed and authorized to charge all required fees, except for the Issue Fee and the Publication Fee, to Deposit Account No. 19-4880. Please also credit any overpayments to said Deposit Account.

Respectfully submitted,



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